

Dual Branch MIM Array Technology for Low-Cost AMLCDs

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Abstract

The three-mask fabrication process and performance of a low cost 10.4 in. VGA Active Matrix LCD using a novel Dual Branch MIM diode pixel circuit is described. The new circuit is insensitive to variations in characteristics of the Si-rich $\text{SiN}_x\text{:H}$ diodes and to RC delays on buslines, as evidenced by circuit measurements and simulations.

Introduction

Metal-Insulator-Metal (MIM) diodes have been investigated as a low cost alternative to TFTs in Active Matrix LCDs since 1980. Anodic Ta_2O_5 [1] and Si-rich siliconnitride deposited by Plasma Enhanced CVD [2,3] have been studied most intensively as the semi-insulator material in MIM diodes. The fabrication of MIM arrays requires a simple process with 2 to 4 photomask steps, as compared to 6 to 9 photomask steps for TFT arrays. Relatively benign design rules for MIM array patterning of 10 μm minimum feature size and 3 μm overlay tolerance (as compared to 4 μm and 1 μm for TFT arrays, respectively) allow the use of low cost, high throughput exposure equipment such as Scanning Projection Aligners [4]. In spite of their low production cost, MIM LCDs have, because of lower image quality, never seriously threatened the dominance of TFT LCDs. A 5-level row drive method was introduced in 1993 [3] to improve gray shade control. We recently described a novel pixel circuit with two branches of MIM diodes and two select lines per row of pixels [5,6]. Circuit modeling indicated that this circuit, when operated in a Simultaneous Scan mode, provides superior gray shade control, response time and tolerance for RC delays on buslines. In this paper we describe fabrication of a prototype display and circuit measurements which support the circuit modeling results.

Device fabrication and measurements

MIM diodes were fabricated using Si-rich siliconnitride ($\text{SiN}_x\text{:H}$) as the insulator. An ITO layer was deposited and patterned first on 350x400 mm Corning 1737 glass substrates. The approximately 1000 \AA thick Si-rich SiN_x layer was then deposited at a

rate of 1500 \AA per minute in an AKT-1600 PECVD system, using a mixture of SiH_4 and N_2 as the precursors. Details of the SiN_x deposition were described in our previous paper [7]. The film properties, including Si/N ratio and film thickness, are tailored to obtain an MIM diode with appropriate ON current, OFF current and capacitance for application in AMLCDs [7]. The SiN_x layer was patterned in islands by dry etching, followed by the deposition and patterning of the Mo top electrode. The device area is defined by the crossover area of the ITO bottom electrode and the Mo top electrode. Figure 1 shows the measured current-voltage characteristics of typical 100x100 μm back-to-back connected diodes at 20, 50 and 80 $^\circ\text{C}$.

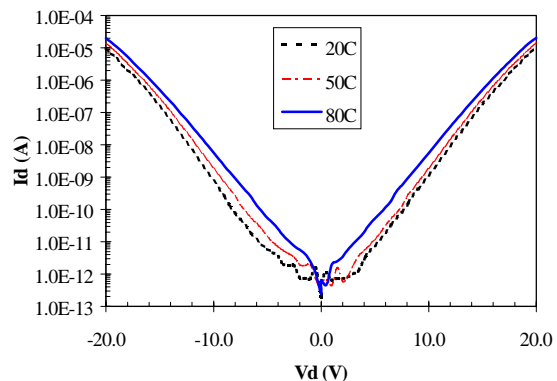


Figure 1. Measured current-voltage characteristics of SiN_x MIM diodes at different temperatures

Circuit measurements

To demonstrate the superior performance of the Dual Branch MIM circuit, pixel charging was measured in test circuits with load capacitors, fabricated simultaneously with the MIM arrays for the displays (figure 2). The voltage V_p at the node between the switching diodes and the load capacitor of 42 pF, representing the pixel voltage, was measured with a high impedance active probe. In figure 3 the measured voltage across the capacitor for both circuits, $V_p - V_d$, is plotted at 20, 50 and 80 $^\circ\text{C}$, corresponding to the current-voltage curves of figure 1.

As predicted by circuit modeling [5], the voltage across the load capacitor, $V_p - V_d$, is much less dependent on variations of the MIM curve with

temperature in the Dual MIM circuit than in the Single MIM circuit. This allows superior gray shade control in LCDs with the Dual MIM circuit, with gray levels that are less dependent on MIM current variations over temperature, across the display area and over time due to device degradation. In addition, pixel charging saturates much better in the Dual MIM circuit and the pixel voltage shift at the end of the select time is eliminated [5].

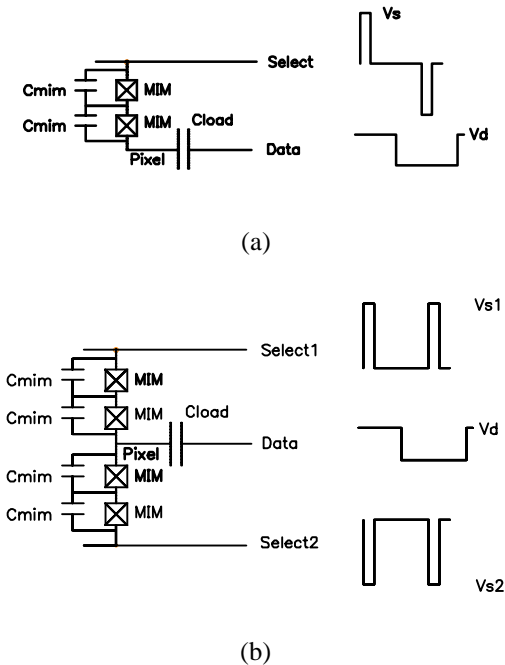


Figure 2. Test circuit for pixel charging in Single MIM circuit (a) and Dual MIM circuit (b)

Display fabrication

The Dual MIM circuit was applied in VGA displays with a diagonal size of 10.4 in. The display has 480x640(x3) pixels with a pitch of 110x330 μm . The three-mask process, described for the test circuit, was used for the MIM array. A two-mask process without any dry etching can also be used [6]. In figure 4 the layout of a group of three pixels is shown. Each pixel contains four 10x10 μm MIM diodes, two back-to-back connected diodes in each branch of the Dual MIM circuit. The twin MIM diodes in each branch serve two purposes. They ensure perfectly symmetric current-voltage curves for each branch and they provide a degree of redundancy in case of a MIM diode short.

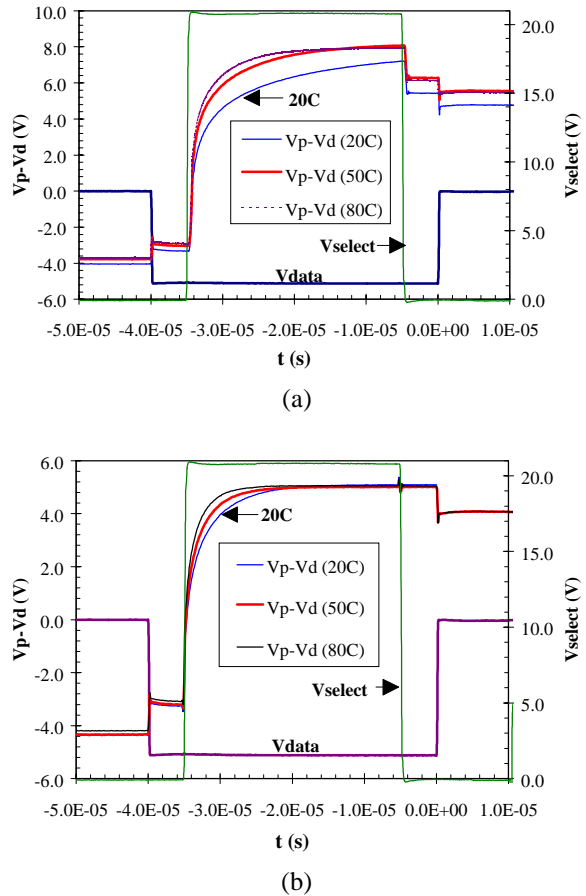


Figure 3. Measured pixel charging in Single MIM circuit (a) and Dual MIM circuit (b) for SiN_x diodes of figure 1

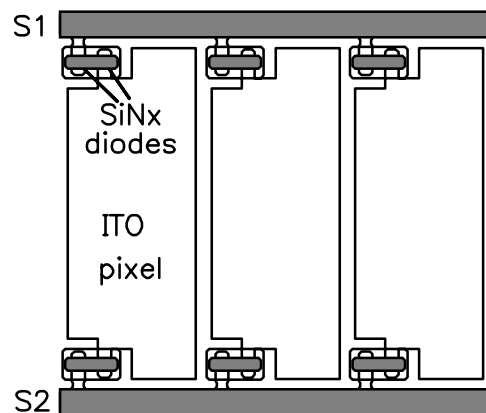


Figure 4. Pixel layout of three pixels in 10.4 in. VGA Dual MIM color LCD

Custom row drive electronics were developed to generate the opposite polarity select pulses at S1 and S2 of each row.

Initial results indicate good gray shade uniformity. The first displays, although research prototypes, had few pixel defects, reflecting the high potential yield with a simple process.

Simulation of 28 in. SVGA displays

In Dual Branch MIM LCD's the pixel voltage is much less dependent on RC delays on buslines than in conventional Single MIM LCD's [5]. SPICE circuit simulations of 28 in. diagonal SVGA displays in both Dual and Single MIM configurations were performed to elucidate the differences. Table I lists the circuit simulation parameters.

TABLE I. CIRCUIT MODELING PARAMETERS FOR 28 IN. DIAGONAL MIM LCDs

Configurations	1.SVGA Vertical stripe Dual MIM, all rows driven from one side 2. SVGA Vertical stripe Single MIM
Pixel count	600 x 800 (x3)
Pixel pitch	720 x 240 μm
Pixel parameters	
MIM I_s (20x20 μm device)	3E-14 A
MIM V_c	0.875
MIM capacitance	0.155 pF (per branch)
LC capacitance	1.7 pF
Array parameters	
Row resistance	Variable - 1 to 4 kohm
Row capacitance	340 pF
Column resistance	Variable - 12 to 48 kohm
Column capacitance	157 pF
Drive waveforms	
Refresh rate	60 Hz
Line time	27 μsec
Select time	24 μsec
Select voltages	+15 and -15 V
Data voltage	+/- 3.5 V

The minimum feature size for the 720 x 240 μm pixel is 20 μm , much larger than the 4 to 6 μm typically used in TFT LCD's. The MIM diode is modeled using the following equation:

$$I = I_s \left[\exp\left(\frac{V}{V_c}\right) - \exp\left(\frac{-V}{V_c}\right) \right],$$

where $I_s = 3\text{E-}14$ A and $V_c = 0.875$ V.

There are large differences between the two circuits. Figures 5 and 6 show 3-dimensional plots of the dependence of pixel voltage variation across the viewing area on row and column resistance for each

circuit. In the Single MIM circuit the pixel voltage variation depends linearly on the busline resistances. Even at the lowest row and column resistance simulated there is 400 mV variation. In the Dual MIM configuration there is an asymptotic dependence of the pixel voltage variation on busline resistance. Pixel voltage variation is very small, less than 50 mV, for $R_{row} < 2$ kohm and $R_{column} < 24$ kohm.

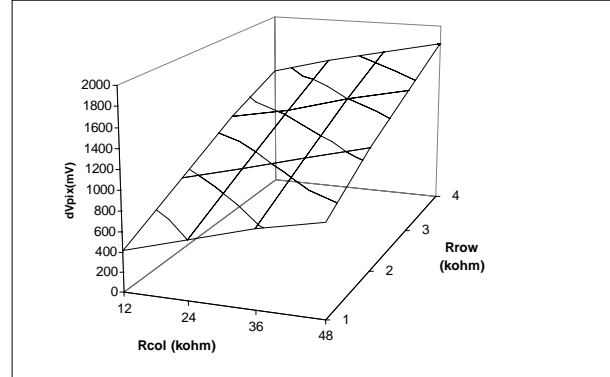


Figure 5. Dependence of pixel voltage variation across 28 in. SVGA Single MIM display on R_{row} and R_{col}

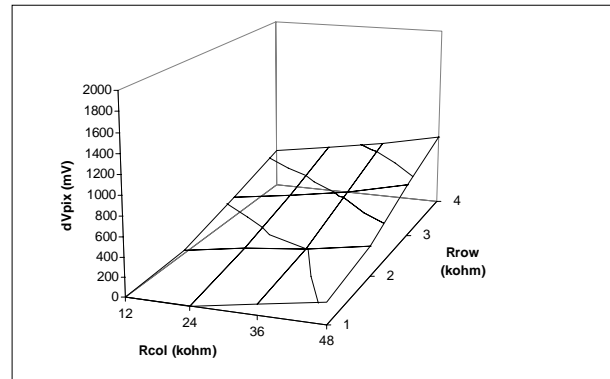


Figure 6. Dependence of pixel voltage variation across 28 in. SVGA Dual MIM display on R_{row} and R_{col}

Discussion

In the Single MIM circuit the pixel voltage V_p at the end of the select time is poorly defined and the result of integration of the MIM current during the select time. The pixel charging never saturates and V_p is given by:

$$V_p = V_{p,-} + \int_0^{t_s} I_{mim} [V_{mim}(t)] dt / C_{lc}$$

where $V_{p,-}$ is the pixel voltage immediately before the select pulse, t_s is the select time, I_{mim} is the MIM current, which depends on the MIM voltage V_{mim} and C_{lc} is the LC capacitance. The MIM voltage is further given by:

$$V_{min}(t) = V_{select}(t) - V_d(t) - V_{lc}(t)$$

The above equations show that the pixel voltage V_p depends on the initial pixel voltage V_{p-} , on the MIM current-voltage characteristics, on C_{lc} (which in turn depends on voltage, time and LC cell gap) and also on the detailed shapes of the select pulse and data pulse. Select and data pulse distortion along the buslines will have a major effect on the pixel voltage.

In the Dual MIM circuit the pixel voltage is independent of the detailed MIM IV curves and independent of the detailed shape of the select and data pulse, as long as pixel charging saturates. When the IV curves of the two branches in the Dual MIM circuit are equal, the pixel voltage at the end of the select time is simply given by:

$$V_p = V_d$$

assuming that $V_{s2} = -V_{s1}$, i.e. the select pulses on the two select lines of one row are equal in magnitude and have opposite polarity. The Dual MIM switch functions as an analogue switch, when operated in a simultaneous select mode, and transfers the data voltage exactly to the pixel, much like a TFT. The pixel voltage shift, proportional to C_{min}/C_{lc} in the Single MIM circuit, is absent in the Dual MIM circuit due to cancellation of the capacitive feedthrough in the two branches.

The two conditions that need to be satisfied for the Dual MIM switch to function as an analogue switch (i.e. $V_p = V_d$) are:

- a. The IV curves of the two branches need to be identical.
- b. $V_{s2} = -V_{s1}$ for each pixel along the row and column lines

Condition a. is met because of the proximity of the MIM diodes in the two branches of one pixel. Although the SiN_x diode IV curves can vary across the display area as a result of temperature variations, SiN_x thickness and composition (e.g. Si/N ratio) variations or variations in the electrode widths, they can be normally assumed not to vary over a few hundred microns within one pixel. Variations in those parameters are canceled out in a Dual MIM circuit.

Condition b. requires the two select voltages to have equal magnitude across the entire display. The load on the rows in the Dual MIM circuit has both a capacitive and a resistive component (as compared to TFT arrays, where the load is purely capacitive as long as the gate nitride is not leaky). The resistive component arises from the current flowing through the MIM diodes from the positive select line to the negative select line even when the pixel is fully charged. This

effect causes a voltage drop in the select pulse amplitude along the row line. When pixel charging saturates, this voltage drop (typically a few hundred mV for a 28 in. display) is equal for the negative and the positive select line, so that the condition $V_{s1} = -V_{s2}$ remains satisfied.

A row resistance of 2 kohm gives good uniformity in the 28 in. Dual MIM SVGA display and corresponds to an Al row busline with a width of 30 μm and a thickness of 0.3 μm . A thicker Al layer of e.g. 1 μm makes even larger displays feasible.

Conclusions

A novel type of low cost MIM LCD has been fabricated with improved gray shade performance. Simulations show that this technology can be scaled up to LCD's with a diagonal size exceeding 28 inches.

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References

- [1] D.R. Baraff, J.R. Long, B.K. McLaurin, C.J. Miner and R.W. Streater, "The Optimization of Metal-Insulator-Metal Nonlinear devices for Use in Multiplexed Liquid crystal Displays", IEEE Trans. Electron Devices, Vol. ED-28, p. 736, 1981
- [2] M. Suzuki, M. Toyama, T. Harajiri, T. Maeda and T. Yamazaki, "A new Active Diode Matrix LCD Using Off-stoichiometric SiN_x layer, Japan Display '86, p. 72
- [3] A.G. Knapp, J.N. Sandoe, J.M. Shannon, P.B.A. Wolfs, J.H.W. Kuntzel and A.J. van Roosmalen, "High Quality TFD-R Video Displays", SID 93 Digest, p. 379
- [4] R.E. Sheets and H.G. Muller, "Scanning Projection Exposure Tools for Large Area Thin Film Displays", Proc. 1994 Display Man. & Techn. Conf., p. 97
- [5] W. den Boer, "A Two-Diode Pixel Circuit and Addressing Method for MIM LCDs", Proc. Eurodisplay '96, p. 25
- [6] W. den Boer, "Balanced Drive Symmetric MIM diode Configuration and Method of Operating Same", European Patent Application EP 0434 627 A2, 1990
- [7] V. Veerasamy, W. den Boer and K. Khan, "Large Area Fabrication of Si-rich SiN_x :H MIM arrays" Proc. Flat Panel Display Strategic Symposium, Ypsilanti, MI, Sept. 97, p. 151