6.2: A Select Line Driver for the Offset-Scan-and-Hold Dual Select Diode AMLCDs

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Abstract

The basic architecture for an offset-scan-and-hold row select driver for Dual Select Diode (DSD) AMLCDs is presented. It can be implemented in a 30 V CMOS process. The performance of the row driver was simulated with SPICE. This drive method eliminates vertical cross-talk and can be used in conjunction with 5 V or 3.3 V data drivers on low cost AMLCDs with diagonal size up to at least 30 in.

1. Introduction

Dual Select Diode (DSD) AMLCDs have recently been proposed [1,2] as a low cost alternative to TFT LCDs for applications ranging from cell phones to large area TV. They have a mode of operation (figure 1) comparable to that of Plasma-addressed LCDs (PALC displays) with pixel electrodes that are reset to a predetermined voltage during each select time, in case of DSD AMLCDs to $(V_{s1}+V_{s2})/2$. The color plate has ITO data-lines and can be identical to that for STN or PALC displays.

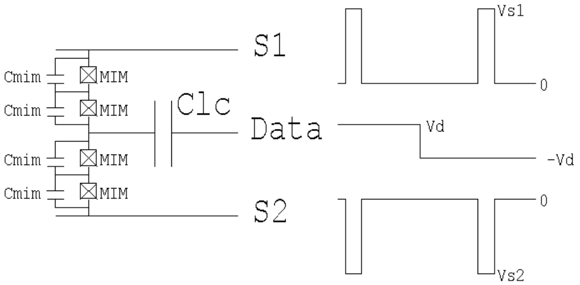

Figure 1. Pixel circuit diagram for DSD AMLCD with basic drive scheme

When the select pulses are terminated, the data voltage is accurately stored on the pixel, due to auto-compensation of the pixel voltage for spatial and temporal variations in the MIM diode current-voltage characteristics [1,2]. DSD AMLCDs can be produced with only two mask steps for the active array and with less than 40 % of the equipment of an a-Si TFT array line. It was also shown by simulation that DSD AMLCDs can be scaled up to very large area exceeding 30 in. [1], as a result of auto-compensation of the pixel voltage for RC delays on buslines.

Figure 2 shows an image on a prototype 10.4 in. VGA color DSD AMLCD, that was developed earlier [1], using two branches of Si-rich SiN_x diodes as pixel switches. Although the performance of this display was very promising, with uniform gray shades and no image retention, some vertical cross-talk was observed for certain test patterns, when using the basic drive scheme of figure 1. Vertical cross-talk in AMLCDs is well understood, both in TFT-based [3] and diode-based [4] displays. In high-resolution displays it occurs even in row inversion drive, i.e. when data polarity is reversed after each line time. In TFT LCDs the vertical cross-talk is caused by pixel-to-dataline capacitances. In displays with two-terminal devices there is an additional contribution to the cross-talk from the diode capacitance, C_{mim} in figure 1. Although this cross-talk can be eliminated by pre-correction of the data signal in hardware [4] or software [3], the drive scheme itself can also be optimized to minimize vertical cross-talk.

To eliminate cross-talk in DSD AMLCDs an offset-scan-and-hold drive method was proposed [5]. This drive method can not be implemented with off-the-shelf AMLCD row drivers. In this paper a basic architecture and circuit simulations for a row select driver with the offset-scan-and-hold feature are presented.

Figure 2. Image on 10.4 in. color VGA DSD AMLCD developed earlier [1] using the basic drive scheme

2. Row select driver architecture

In the offset-scan-and hold drive method for DSD AMLCDs both V_{s1} and V_{s2} are offset by a holding voltage V_h between +/- 1 to 3 V. The holding voltage has opposite polarity for odd and even rows and for odd and even frames. During the non-select period the select lines are held at the corresponding holding voltages.

In figure 3 the basic architecture of two stages in the offset-scan-and-hold driver is shown. They drive the select lines S_{1i}, $S_{2,i}$, $S_{1,i+1}$, $S_{2,i+1}$ of two adjacent rows. A four-phase shift register SR, which selects one-row-at-a-time addressing, drives two edge-triggered flip-flops FF. The D input of FF is generated by the FF output of a preceding FF. The flip-flops generate the transitions to the four voltage levels required for each of the S_1 and S_2 select lines of one row. Four level shifters LS, two for S_1 and two for S_2, raise the voltage range to that required for the positive select pulse at S_1 and the negative select pulse at S_2, respectively. Finally, two 4x multiplexers MUX are used to apply the select and holding voltages to the S_1 and S_2 select lines. The size of the p-channel and n-channel transistors in the multiplexer are adjusted to obtain matching output impedance. The row driver can be implemented in a 30 to 35 V CMOS process.

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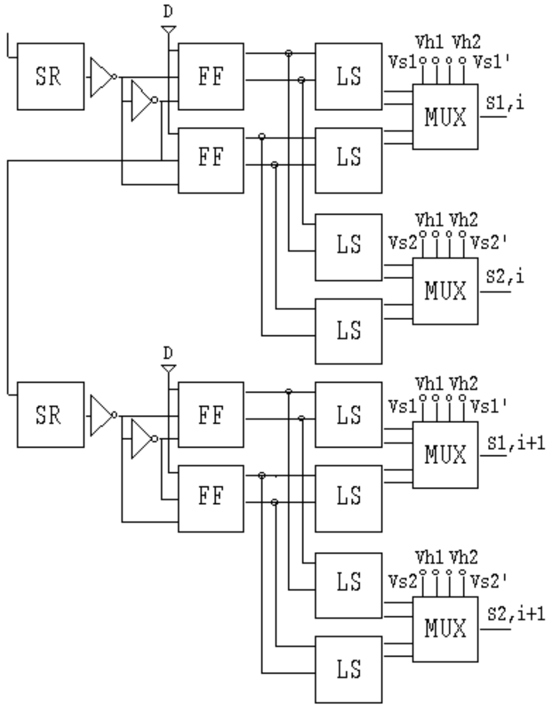

Figure 3. Basic architecture of two stages of the offset-scan-and-hold row driver

The row driver performance was simulated using SPICE. In figure 4 the four outputs to drive S_1 and S_2 of two adjacent rows are shown. The 6 input voltages to the MUX determine the holding voltages V_{h1} and V_{h2} and the select voltages V_{s1} and $V_{s1'}$ on S_1 and V_{s2} and $V_{s2'}$ on S_2. The use of the edge-triggered flipflop FF allows the holding voltages to extend beyond the frame time, until the line is selected again. V_{s1}, $V_{s1'}$, V_{s2} and $V_{s2'}$ were 12, 18, -18 and -12 V, respectively, in the simulation shown in figure 4, while V_{h1} and V_{h2} were 3 V and –3 V . In general, it is advantageous to chose the select voltages to be offset by the holding voltage with respect to a center value, in this case 15 V. This eliminates a pixel voltage shift at the end of the select time by complete cancellation of the capacitive feed-through voltages from the diode capacitances. The line time was 20 μsec and equal to the select time and the frame time was shortened to 100 μsec in order to show two select times in the plots.

The holding voltages have opposite polarity for row i and row i+1, so that row inversion (inversion of the data-signal polarity per line time) can be used to eliminate flicker. Like V_{com} modulation drive in TFT LCDs, the offset-scan-and-hold drive method is only compatible with row inversion, not with column or dot inversion. It allows, however, the use of low voltage data drivers, as low as 3.3 V when a low threshold LC fluid is employed. Even for very large DSD AMLCDs with diagonal size exceeding 30 in. data drivers with a total swing of 3.3 V are feasible, thereby further reducing overall cost.

The holding voltage is typically chosen to be about 0.5 V above V_{50}, the voltage at which the transmittance of the LC cell is 50 % of its maximum value. For example, the voltage across the LC can vary from 1 V to 4.3 V when a 3.3 V data driver is used in combination with a holding voltage of 2.65 V.

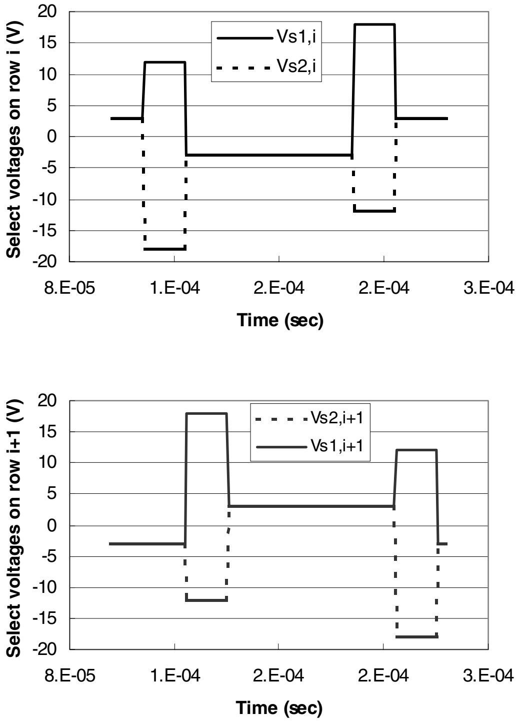

Figure 4. Simulated output waveforms on S1,i, and S2,I (top), and S1,i+1 and S2,i+1 (bottom) of the row driver

It was shown earlier by analytical calculations [5] that the offset-scan-and-hold drive method virtually eliminates vertical cross-talk in DSD AMLCDs.

A major additional advantage of the offset-scan-and-hold drive method is that the voltage across the MIM diode during the non-select period is much lower than with the basic drive scheme [5].

The Si-rich SiN_x layer used in the display of figure 2 as the semi-insulator in the MIM diode has a bottom electrode of ITO and can therefore be exposed to rather high light intensity. Although the photoconductivity of Si-rich SiN_x is many orders of magnitude lower than that of amorphous silicon, a photoleakage current can be observed in the current-voltage curves as shown in figure 5 for a device consisting of two series-connected diodes. In the prototype with the basic drive scheme photo-leakage currents, which can affect charge holding on the pixel, were suppressed by operating the display with the transparent ITO bottom electrode facing the viewer and the color plate facing the backlight.

When using the offset-scan-and-hold drive method with 5 V data drivers, the operating regime of the diode during the non-select period is much smaller [5]. Charge loss from the pixel through the diode is then expected to be negligible, even in the presence of a photo-leakage current, as illustrated in figure 5.

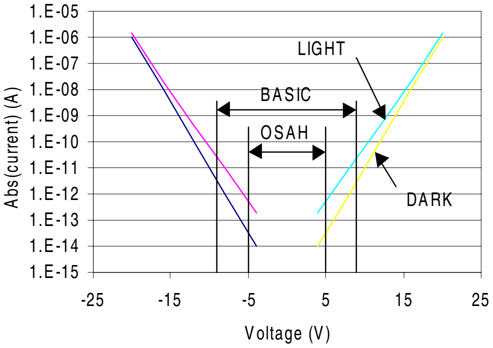

Figure 5. Maximum operating regime of SiN$_x$ diode in non-select state for BASIC and offset-scan-and-hold (OSAH) drive with 5 V data swing

3. Display process considerations

A key advantage of the DSD AMLCD, in addition to the small number of process steps for the Active Matrix array, is the scaling of design rules for photo-patterning [6]. For TFT LCDs the minimum feature size and overlay requirements are approximately the same for a 10 in. and a 40 in. SVGA display (at 4 µm and 1 µm, respectively). For a DSD AMLCD they are already relaxed at 10 in. size (10 µm and 3 µm, respectively) and scale for 40 in. size to 40 µm and 12 µm, respectively. The scaling is the result of the vertical current flow in a two-terminal device, which has a side dimension proportional to the pixel pitch. In a TFT, on the other hand, current flow is lateral and the channel width of the TFT is proportional to the square of the pixel pitch, while the channel length (the minimum feature size) and the gate/source overlap (which determine overlay requirement) do not change significantly with pixel pitch.

The greatly relaxed design rules for patterning DSD arrays allow, in principle, the use of single shot, low cost magnification exposure equipment in combination with standard size masks used in the semiconductor industry. In Table I the process steps for the DSD AMLCD and the a-Si TFT LCD are compared.

Table I. Comparison of process steps for a-Si TFT arrays and DSD arrays

	a-Si TFT array	DSD array
PECVD steps	4 to 5	1
Dry etch steps	3 to 5	0 or 1
Sputtering steps	3 to 4	2
Photolithography:		
steps active array	≥ 5	2 or 3
resolution	4 µm	≥ 10 µm
overlay accuracy	1 µm	≥ 3 µm
equipment	Flat panel steppers	Scanning projectors, proximity printers or magnification exposure equipment

The display shown in figure 2 was made with three photo-steps [1] by depositing and patterning ITO first, followed by deposition and patterning of the SiN$_x$ layer and deposition and patterning of the metal (Mo) for select lines and top electrodes of the MIM diodes. The diode dimensions are determined by the cross-over area of ITO and Mo. A two-mask process can also be used by leaving the SiN$_x$ layer un-patterned or by patterning the metal layer and the SiN$_x$ layer in the same step. The small number of process steps could allow in-line rather than batch processing and minimizes cycle time and manufacturing cost. In addition, when conventional flat panel steppers and mirror projection aligners can be replaced by lower cost exposure equipment, manufacturing cost for the array is further reduced. The DSD AMLCD does not have crossing buslines on the same substrate, which is expected to improve yield.

There is only one PECVD step in the entire process (for the SiN$_x$ layer with a thickness of about 100 nm). It has a deposition time of about 40 seconds in standard AKT PECVD equipment. Since the metal top electrode covers the diode, a passivation layer is not required.

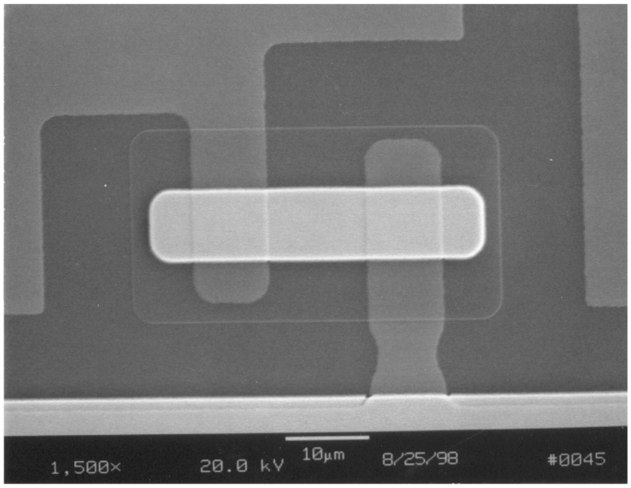

Figure 6. SEM micrograph of one branch of SiNx diodes in the DSD pixel layout

In figure 6 an SEM micrograph is shown of one branch of the DSD pixel layout with two 10x10 µm SiN$_x$ diodes. At the bottom of the micrograph one of the two select lines is shown, which, for redundancy purposes, consist of both ITO and metal (Mo). The use of twin diodes in each branch of the Dual Select circuit ensures symmetric current-voltage characteristics.

Care should be taken to prevent the reduction of ITO in the hydrogen containing plasma during SiN$_x$ layer deposition, which leads to a cloudy appearance of the SiN$_x$ layer on ITO and poor device reliability. By optimizing the SiN$_x$ deposition recipe this problem was solved and reliable, reproducible SiN$_x$ MIM diodes were fabricated. Device reliability is also affected by the ITO thickness. Diode breakdown typically occurs at the edge of the ITO pattern and an ITO layer with a thickness less than the SiN$_x$ layer thickness increases the breakdown voltage.

The bi-directional non-linear conduction in the SiN$_x$ diode is key for the operation in the LCD. It is believed to be dominated by Frenkel-Poole conduction, based on its dependence on voltage and temperature and on the scaling with SiN$_x$ layer thickness [7].

4. Display performance considerations

The pixel voltage in DSD AMLCDs is not much affected by long range variations of the SiN_x diode characteristics and by RC delays on buslines, both as a result of the auto-compensation effect in the pixel circuit, as shown in circuit simulations [1,2].

For very large displays, however, the RC delay on the buslines can still play a role and low resistivity row select buslines are required. In the DSD AMLCD a thick Al layer of e.g. 0.5 or 1 µm can be used for the select lines, since it is the last layer in the array process and, as there are no crossing buslines on the same substrate, there is no concern about step coverage.

SiN_x diodes are known for a gradual degradation of the ON current after prolonged operation. This can lead to image retention in conventional single branch diode pixel circuits. In the DSD pixel circuit both branches of diodes within one pixel will degrade the same over time, although the degradation can vary from pixel to pixel depending on the image displayed. Since the DSD circuit will retain its balanced drive operation, image retention is expected to be absent. Indeed, the prototype display did not show image retention. The DSD switch is a three-terminal device and functions as an analog switch. Like a TFT, it accurately charges the pixel to the data voltage, regardless of some variations in the device characteristics over time or across the display area.

The DSD AMLCD does not have a storage capacitance at each pixel. The main function of a capacitor in TFT LCDs is to suppress the effects of asymmetric, gray-level dependent pixel voltage shifts when the gate is switched OFF. There is no pixel voltage shift in DSD AMLCDs when the diodes are switched off as a result of the cancellation of capacitive feed-through voltages from the two opposite polarity select pulses. A capacitor is therefore less needed in a DSD AMLCD.

The two select lines per row in the DSD pixel array require twice the number of external row driver connections. In displays with a vertical stripe pixel arrangement this adds 15 to 20 % to the total number of interconnects (depending on the aspect ratio of the display: 4:3 or 16:9). The added interconnects are on the "easy" row side with the lower interconnect density. Increased row driver cost is small compared to cost reductions in the Active Matrix array process, especially for larger displays.

As far as optical performance is concerned, the DSD AMLCD is compatible with some methods for viewing angle enhancement, such as Patterned Vertical Alignment (PVA) [8]. Since the ITO on the color plate is already patterned in DSD AMLCDs, no extra processing is required to implement PVA.

The pixel aperture for the prototype display was 50 % using conservative design rules. A high aperture, low reflectance version of the DSD AMLCD, with color filters integrated on the active array, has recently also been proposed [9]. It combines the functions of low reflectance black matrix, select line and bottom electrode for the MIM diode in the same film stack. The high aperture version can increase brightness by 20 to 60 % depending on resolution and further reduces the combined number of mask steps for top and bottom substrate of the color display to six .

For resolutions higher than SVGA or XGA the ON/OFF current ratio of SiN_x diodes may not be high enough. Other semi-insulator materials such as diamond-like carbon or carbon-nitride have potential for diodes with higher ON/OFF current ratios and lower diode capacitance [5].

5. Summary

A row select driver architecture for the offset-scan-and-hold drive in DSD AMLCDs has been presented. The drive method is expected to eliminate vertical cross-talk and improve charge retention on the LC pixel capacitance.

DSD AMLCD technology is based entirely on existing infrastructure for AMLCD equipment, materials and low voltage data drivers. The prototype shown in figure 2 was made on a TFT LCD line using only a small fraction of the array equipment. With a reduced number of process steps the manufacturing yield, an overriding factor determining cost, is expected to be higher than for TFT LCDs. If further developed, the performance of DSD AMLCDs could match or approach that of TFT LCDs, but at lower manufacturing cost. Therefore, the DSD AMLCD is a promising alternative technology in the rapidly expanding market for AMLCDs. In particular for large size applications, such as LC TVs, where TFT LCDs are still prohibitively expensive, the DSD AMLCD may provide a lower cost option.

6. References

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